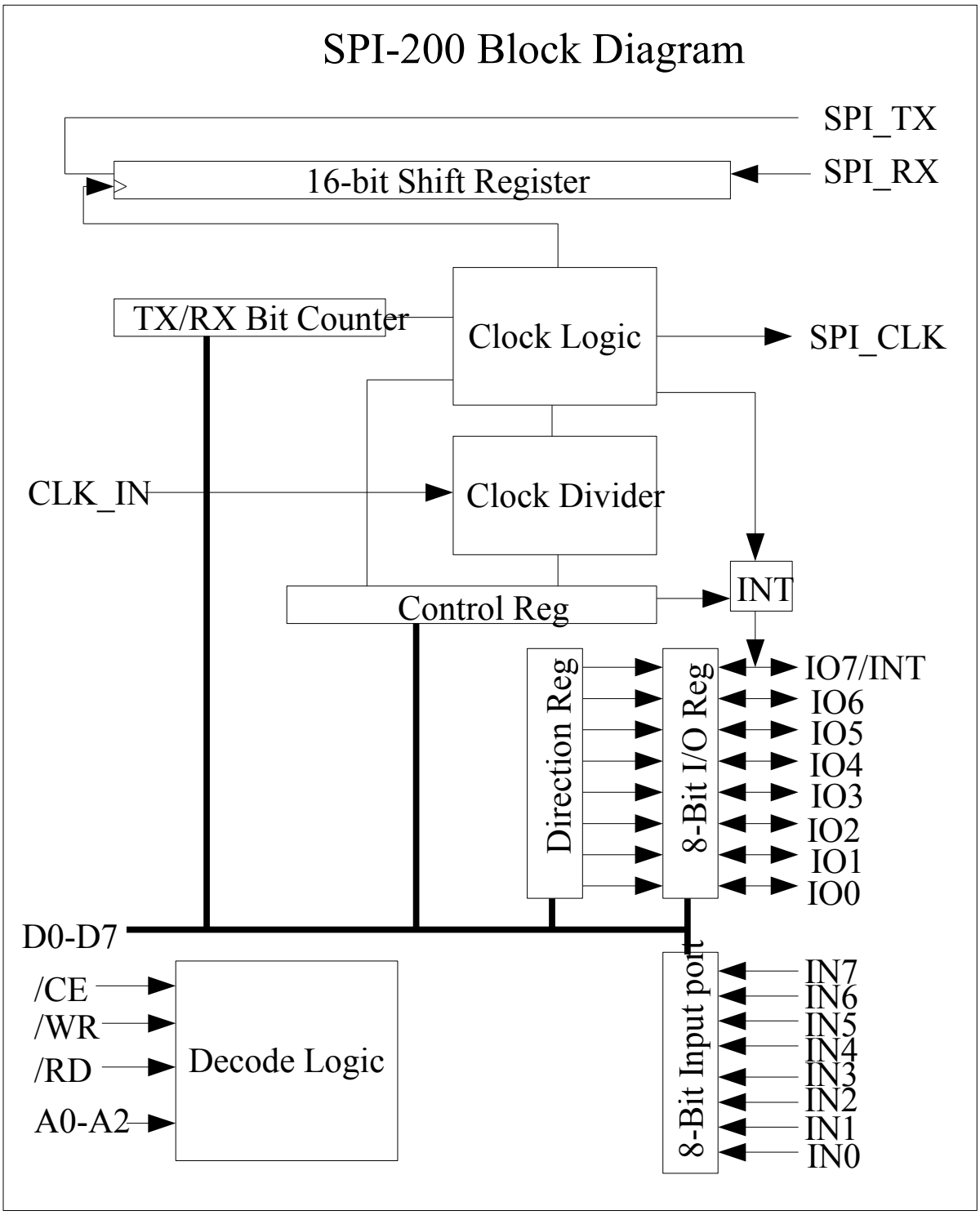
SPI-200 Master SPI Controller

Revised 8-24-2006



1.0 Description

The SPI-200 chip provides a high-speed SPI master controller and bit I/O.

Features:

- High-speed up to 25MBit/sec.
- 16-bit serial data register.
- Programmable Transmit Length from 1 to 31 bits.
- Programmable clock polarity.
- Programmable input clock edge.
- Programmable output clock edge.
- Programmable RX polarity.
- 8-bit Input or Output port, each pin has programmable direction.
- 8-Bit input port.
- 3.3V power, 5V tolerant I/O.
- Small PLCC-44 or PQFP-44 package.
- MSB-first out (no need for software bit reversal.)
- Programmable clock divider From CLK_IN/2 to CK_IN/256.
- I/O interface compatible with most processors.
- Programmable interrupt output.

The SPI-200 is designed to support any SPI device. The programmable clock polarity and in/out clock edge options allow any SPI mode to be implemented.

The IO ports ca be used for chip select signals to allow multiple SPI devices to share one SPI bus.

Pin descriptions

Pin # PQFP	***Pin # PLCC***	***Name***	***Description***	***Direction***
1	7	CLK_IN	Master Clock 0-50MHz	Input
2	8	A0	Address	Input
3	9	A1	Address	Input
4	10	GND	Ground	
5	11	A2	Address	Inp
6	12	SPI_DO	SPI Data Out	Output
7	13	SPI_DI	SPI Data In	Input
8	14	SPI_CLK	SPI Clock	Output
9	15	TDI	JTAG Port (no Connection)	Input
10	16	TMS	JTAG Port (no Connection)	Input
11	17	TCK	JTAG Port (no connection)	Input

Pin # PQFP	***Pin # PLCC***	***Name***	***Description***	***Direction***
12	18	IN0	Input Port bit 0	Input
13	19	IN1	Input Port bit 1	Input
14	20	IN2	Input Port bit 2	Input
15	21	VCC	Power	
16	22	IN3	Input port bit 3	Input
17	23	GND	Ground	
18	24	IN4	Input Port bit 4	Input
19	25	IN5	Input Port bit 5	Input
20	26	IN6	Input Port bit 6	Input
21	27	IN7	Input Port bit 7	Input
22	28	IO7/INT	IO port bit 7, INT output	I/O
23	29	IO6	IO Port bit 6	I/O
24	30	TDO	JTAG Port (no connection)	Output
25	31	GND	Ground	
26	32	VCC	Power	
27	33	IO5	IO Port bit 5	I/O
28	34	IO4	IO Port bit 4	I/O
29	35	IO3	IO Port bit 3	I/O
30	36	IO2	IO Port bit 2	I/O
31	37	IO1	IO Port bit 1	I/O
32	38	IO0	IO Port bit 0	I/O
33	39	D7	Data Bus Bit 7	I/O
34	40	D6	Data Bus Bit 6	I/O
35	41	VCC	Power	
36	42	D5	Data Bus Bit 5	I/O
37	43	D4	Data Bus Bit 4	I/O
38	44	D3	Data Bus Bit 3	I/O
39	1	D2	Data Bus Bit 2	I/O
40	2	D1	Data Bus Bit 1	I/O
41	3	D0	Data Bus Bit 0	I/O

Pin # PQFP	*Pin # PLCC*	*Name*	*Description*	*Direction*
42	4	/CE	Chip Enable	Input
43	5	/RD	Read enable (active low)	Input
44	6	/WR	Write strobe (Active low)	Input

Maximum ratings:

Power Voltage	4.0V Maximum, 3.3v typical, 3.0V Minimum
CLK_IN	0 to 50MHz
IO Pin Current	Source 4MA, Sink 8MA
Input Voltage	0-5V

2.0 Registers

Address	*Register*
0	Shift register bits 15..8
1	Shift Register bits 7..0
2	Transmit Counter
3	Control Register
4	IO port Data
5	IN port Data
6	Version, currently 00000001
7	I/O Port Data Direction Register.

2.1 Shift register

The shift register is 16-bit. It can be used to transmit from 1 to 16 bits in one transfer. Bit 15 is shifted out first and data is sifted in to bit 0.

When using less than 16-bits the data to transmit should be loaded in the upper bits of the register. The data will be clocked into the lower bits.

There are two register addresses to access the shift register. The low and high bytes can be loaded separately.

Note: The shift register is actually 17-bits. Writes are to bits 16-1 and reads are from 15-0. So, data written will be 1-bit off if read back.

The two data registers are set up for little-endian systems. A 16-bit write to address 0 will align the bytes correctly. The low byte will be put in bits 15-8 and sent first. This is to optimize byte

block transfers. To send a 16-bit word, the bytes would have to be reversed.

2.2 Transmit Counter

The control register is an 8-bit register:

7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
SPI_DI	SPI_CLK	BUSY	COUNT4	COUNT3	COUNT2	COUNT1	COUNT0

The transmit counter is a 5-bit write register. Writing any non-0 value to this register will start data transmission. The counter will decrement as each bit is transmitted/received.

Note: a write to the transmit counter forces SPI_OUT to the idle state.

A value from 1 to 31 can be written to the register. Writing 0 will cancel any running transfer. Values greater than 16 are useful for don't care conditions.

Read will return the count and the following signals:

SPI_DI - Current state of the SPI_DI pin

SPI_CLK - Current stet of the SPI_CLK pin

BUSY - 1 if a transfer is in progress.

To test if a transfer is complete it is best to read the Transmit Counter register and and with 0x7f. Any non-0 value will indicate a transfer is in progress.

2.3 Control Register

The control register is an 8-bit register:

7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
TX_FF	TX_EDGE	OUT7/INT	CLK_INV	RX_EDGE	DIV2	DIV1	DIV0

The Control register is read/write.

The DIV bits set the clock rate for the SPI_CLOCK:

DIV2	*DIV1*	*DIV0*	*Rate*
0	0	0	CLK_IN/2
0	0	1	CLK_IN/4
0	1	0	CLK_IN/8
0	1	1	CLK_IN/16
1	0	0	CLK_IN/32
1	0	1	CLK_IN/64

DIV2	*DIV1*	*DIV0*	*Rate*
1	1	0	CLK_IN/128
1	1	1	CLK_IN/256

RX_EDGE 1 - SPI_RX data is sampled on rising edge of SPI_CLK

0 - SPI_RX data is sampled on falling edge of SPI_CLK

CLK_INV 0 - Normal SPI_CLOCK (idle=low)

1 - Inverted SPI_CLOCK (idle=high)

OUT7/INT 0 - OUT7 operates as I/O pin

1- OUT7 is INT output.

TX_EDGE 0 - Data is clocked out on the rising edge of SPI_CLK

1- Data is clocked out of the falling edge of SPI_CLK

TX_OE 0 – SPI_TX Output enabled

1 – SPI_TX output tristate

When set as an INT output, OUT7 will be asserted high when the TX counter is non-0. When operated as an INT pin, it must be set as an output in the IO Data Direction Register.

2.4 IO Port Registers

There are two registers for the output port. On power-up, the pins are set as inputs.

The IO Data register is read/write. Read will return the state of the pins.

IO Port Data Register

7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
IO7/INT	IO6	IO5	IO4	IO3	IO2	IO1	IO0

The IO Port Direction register sets the direction. When 0, the pin is a input; when 1 the pin is an output.

IO Port Data Direction Register: 1=out, 0=input

7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
IO7/INT	IO6	IO5	IO4	IO3	IO2	IO1	IO0

Writes to the data register are stored internally. When a pin is switched from input to output, it will output the last data written.

The IO7/INT pin must be programmed as an output when used as an INT pin.

2.5 IN Port Register

The IN port register will return the current state of the IN pins.

IN Data Register

7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

3.0 Programming

3.1 Variable Bit Transfer

SPI devices usually use multiples of 8 bits. Some use an odd number of bits that force implementing the SPI by bit-banging I/O bits.

The SPI-200 can use any number of bits from 1 to 16. Longer transfers can be done via multiple transfers with the chip select active.

This variable transmit/receive size has an advantage. One use is to transfer a single bit until a start bit is received. Then transfer bytes.

Another option is when a device subdivides a block of data in bit fields. An example may be a memory device with a 14-bit page address and a 10-bit address with in the page. Instead of formatting a 24-bit as bytes, the two fields can be sent as a 14-bit and then a 10-bit transfer.

When sending data, the bits must be left-justified in the shift register.

3.2 SPI Modes

Programming information on specific SPI modes TBD.

3.3 Transfers

The sequence for transmitting or receiving data:

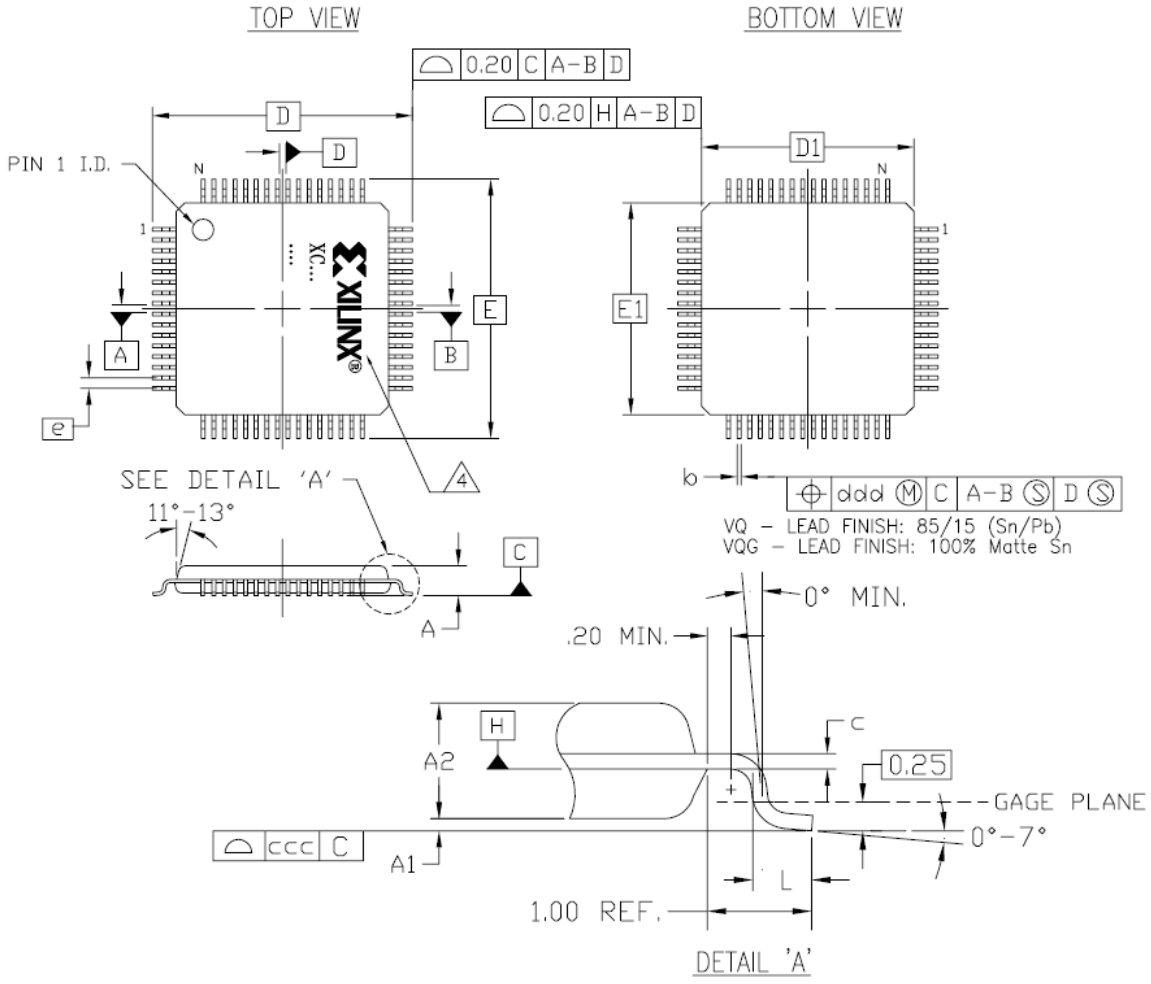
1. Write data to the Shift Data Registers, MSB aligned with bit 15.
2. Write the number of bits to transfer to the Transmit Count Register.
3. Wait for the lower 7 bits of the Transmit Count Register to return to 0 or the falling edge of INT pin.
4. Read the RX bits from Shift Data Register.

4.0 Timing

TBD

5.0 Packaging

PQFP-44:



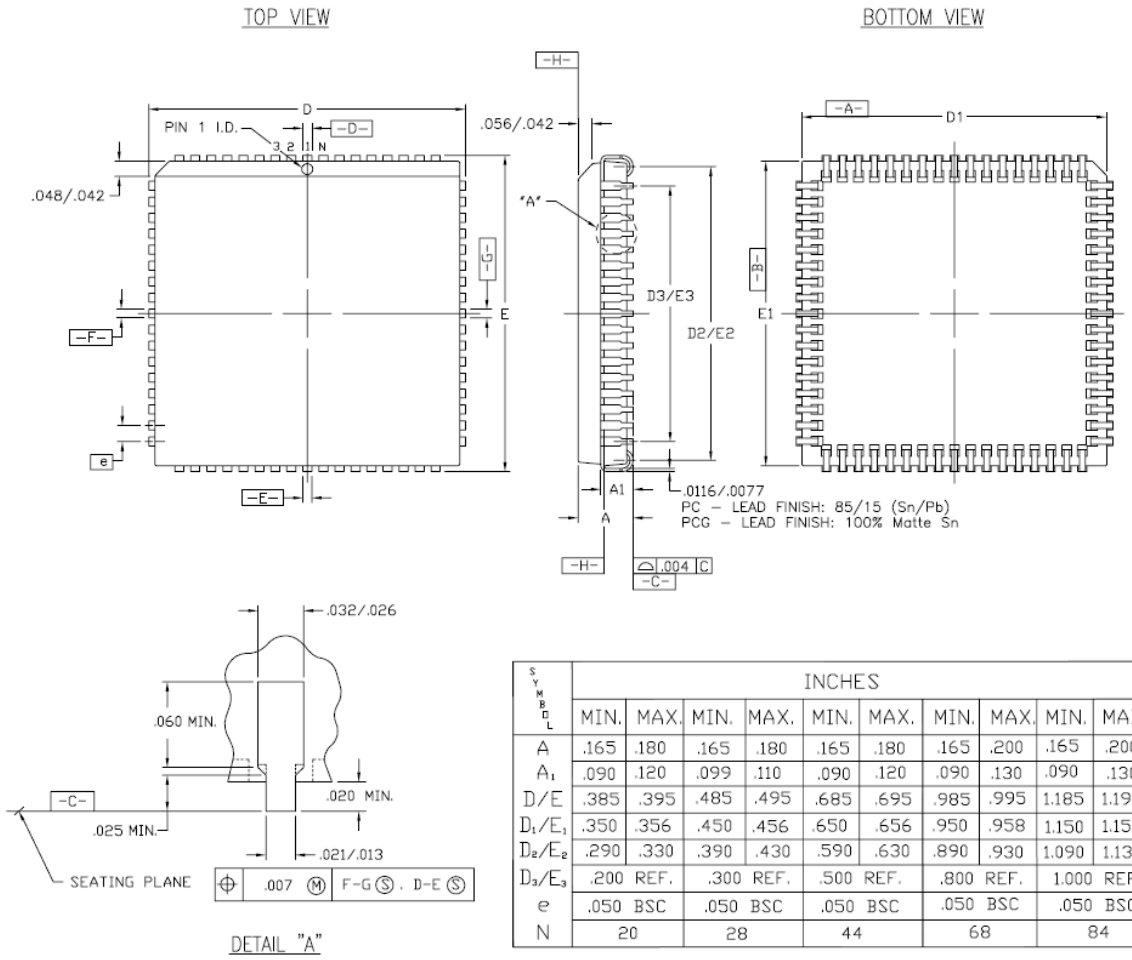
SYMBOL	VQ/VQG44 MILLIMETERS			VQ/VQG64 MILLIMETERS			VQ/VQG100 MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			1.20			1.20
A_1	0.05		0.15	0.05	0.10	0.15	0.05	0.10	0.15
A_2	0.95	1.00	1.05	0.95	1.00	1.05	0.95	1.00	1.05
D/E	12.00 BSC			12.00 BSC.			16.00 BSC.		
D_1/E_1	10.00 BSC			10.00 BSC.			14.00 BSC.		
b	0.30	0.37	0.45	0.17	0.22	0.27	0.17	0.22	0.27
c	0.09		0.20	0.09		0.20	0.09		0.20
e	0.80 BSC.			0.50 BSC.			0.50 BSC.		
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
ccc			0.10			0.08			0.08
ddd			0.20			0.08			0.08
N	44			64			100		
REF.	JEDEC MS-026-ACB			JEDEC MS-026-ACD			JEDEC MS-026-AED		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
3. THE TOP OF THE PACKAGE MAY BE SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15mm.
4. MARK ORIENTATION WITH RESPECT TO PIN–1 I.D. IF 2 OR MORE CIRCLES EXIST ON TOP OF THE PACKAGE, USE THE SMALLEST CIRCLE AS PIN–1 I.D.

44, 64, and 100–PIN PLASTIC VERY THIN QFP
(VQ44/VQG44, VQ64/VQG64, and VQ100/VQG100)

PLCC-44:



SYMBOL	INCHES									
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	.165	.180	.165	.180	.165	.180	.165	.200	.165	.200
A_1	.090	.120	.099	.110	.090	.120	.090	.130	.090	.130
D/E	.385	.395	.485	.495	.685	.695	.985	.995	1.185	1.195
D_1/E_1	.350	.356	.450	.456	.650	.656	.950	.958	1.150	1.158
D_2/E_2	.290	.330	.390	.430	.590	.630	.890	.930	1.090	1.130
D_3/E_3	.200 REF.		.300 REF.		.500 REF.		.800 REF.		1.000 REF.	
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
N	20		28		44		68		84	

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE.
3. 'N' IS NUMBER OF TERMINALS.
4. CONFORM TO JEDEC MO-047
5. TOP OF PACKAGE MAY BE SMALLER THAN BOTTOM BY .010".